



TROUBLESHOOTING GUIDE

**Complete with Signatures
and Memory Map**

Tempest™ Troubleshooting Guide

Complete with Signatures and Memory Map

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NOTE

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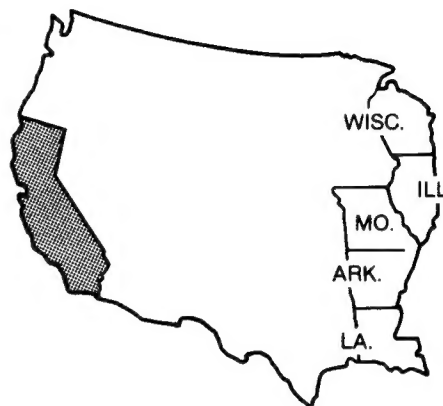
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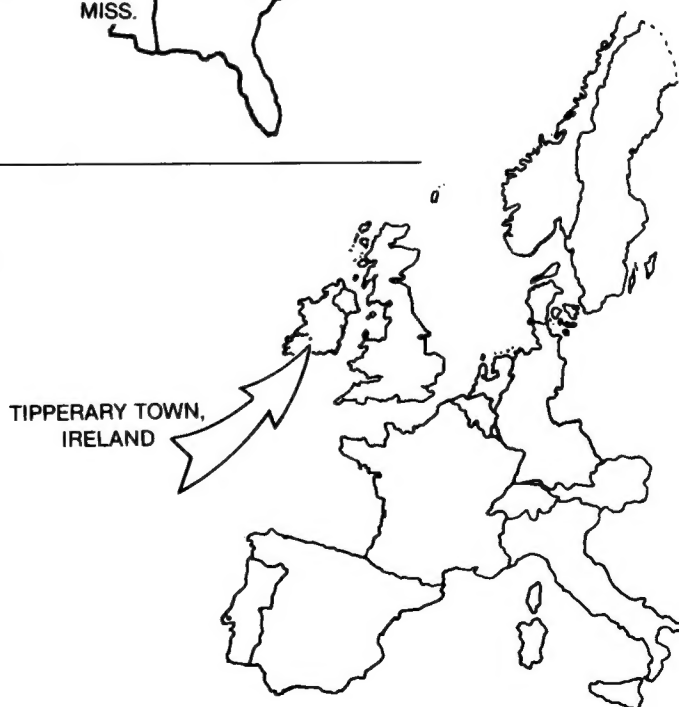
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1 Memory Map

| MEMORY MAP | | | | | | | | | | |
|-----------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---|
| HEXA- DECIMAL ADDRESS | R/W | DATA | | | | | | | | FUNCTION |
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0000-7FFF 0800-080F | R/W W | D | D | D | D | D | D | D | D | Program RAM (2K) Color RAM |
| 0C00 | R | | | | | | | | D | Right Coin Switch |
| 0C00 | R | | | | | | | D | | Center Coin Switch |
| 0C00 | R | | | | | | D | | | Left Coin Switch |
| 0C00 | R | | | | | D | | | | Slam Switch |
| 0C00 | R | | | | D | | | | | Self-Test Switch |
| 0C00 | R | | | D | | | | | | Diag,Step Switch |
| 0C00 | R | | D | | | | | | | HALT |
| 0C00 | R | D | | | | | | | | 3KHz |
| 0D00 | R | D | D | D | D | D | D | D | D | Option Switch Inputs |
| 0E00 | R | D | D | D | D | D | D | D | D | Option Switch Inputs |
| 2000-2FFF 3000-3FFF | R/W R | D | D | D | D | D | D | D | D | Vector RAM (4K) Vector ROM (4K) |
| 4000 | W | | | | | | | | D | Right Coin Counter |
| 4000 | W | | | | | | | D | | Center Coin Counter |
| 4000 | W | | | | | D | | | | Video Invert X |
| 4000 | W | | | | D | | | | | Video Invert Y |
| 4800 | W | | | | | | | | | VG GO |
| 5000 | W | | | | | | | | | WD CLEAR |
| 5800 | W | | | | | | | | | VG Reset |
| 6000-603F 6040 6040 6050 | W W R R | D D D D | D D D D | D D D D | D D D D | D D D D | D D D D | D D D D | D D D D | EAROM Write EAROM Control Math Box Status EAROM Read |
| 6060 6070 6080-609F | R R W | D D D | D D D | D D D | D D D | D D D | D D D | D D D | D D D | Math Box Read Math Box Read Math Box Start |
| 60C0-60CF 60D0-60DF | R/W R/W | D D | D D | D D | D D | D D | D D | D D | D D | Custom Audio Chip 1 Custom Audio Chip 2 |
| 60E0 60E0 60E0 | R R R | | | | | | | D | D | One Player Start Two Player Start FLIP |
| 9000-DFFF | R | D | D | D | D | D | D | D | D | Program ROM (20K) |

Figure 1 Memory Map

2 Watchdog

The Watchdog circuit will cause continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the reset line.

RESET—microprocessor input (pin 40). In a properly operating game, reset should occur during power-up or when the reset push button is activated. A pulsing reset line indicates that something is causing the microprocessor to lose its place within its program. Typical causes are:

1. Open or shorted address or data bus lines
2. Bad microprocessor chip
3. Bad bus buffers
4. Bad ROM
5. Bad RAM
6. Any bad input or output that causes an address or data line to be held in a constant high or low state

A pulsing RESET signal indicates a problem exists somewhere within the microprocessor circuitry rather than within either the Math Box or the Analog Vector Generator.

3 Troubleshooting

Using the CAT Box

A. CAT Box Preliminary Set-up

1. Remove:

- The electrical power from the game.
- The wiring harnesses from the game PCBs.
- The main and auxiliary boards from the game cabinet.
- The microprocessor chip C2 from the main PCB.

2. Connect:

- The harnesses from the game to the main and auxiliary boards. (Use extender cables if available.)
- $\Phi 0$ and $\Phi 2$ test points together.
- W DOG DIS test point to ground.
- The CAT Box flex cable to the main PCB test edge connector.

3. Power Up:

- The game.
- The CAT Box.

4. Set CAT Box Switches:

- TESTER SELF-TEST: (OFF)
- TESTER MODE: R/W
- Press TESTER RESET

B. Address and Data Lines

NOTE: This section assumes that IC F2 is a 74LS245.

1. Perform the CAT Box preliminary set-up.
2. Connect the DATA PROBE to the CAT Box and the game ground test point.
3. TESTER MODE: R/W

4. BYTES: 1.
5. PULSE MODE: UNLATCHED
6. R/W MODE: (OFF)
7. R/W to WRITE
8. Key in address pattern on the keyboard (*use AAAA to start*)
9. Push DATA SET
10. Key in data pattern on the key board (*use AA to start*)
11. R/W MODE: STATIC
12. Probe the IC-pin with the data probe and check for the 1 or 0 LED as indicated in Figure 2. Repeat this step for each address and data line.
13. Repeat steps 6-11 using 5555 in step 8 and 55 in step 10.

Figure 2 Address and Data Lines

| When writing AAAA pattern | Address and data lines | When writing 5555 pattern |
|------------------------------|---------------------------|------------------------------|
| Logic State | IC-Pin | Logic State |
| 1 | B3-1 | 0 |
| 0 | B3-3 | 1 |
| 1 | B3-2 | 0 |
| 0 | A/B-3 | 1 |
| 1 | A/B-18 | 0 |
| 0 | A/B-16 | 1 |
| 1 | A/B-14 | 0 |
| 0 | A/B-12 | 1 |
| 1 | B/C-3 | 0 |
| 0 | B/C-5 | 1 |
| 1 | B/C-7 | 0 |
| 0 | B/C-9 | 1 |
| 1 | B/C-18 | 0 |
| 0 | B/C-16 | 1 |
| 1 | B/C-14 | 0 |
| 0 | B/C-12 | 1 |
| 1 | F2-9 | 0 |
| 0 | F2-8 | 1 |
| 1 | F2-7 | 0 |
| 0 | F2-6 | 1 |
| 1 | F2-5 | 0 |
| 0 | F2-4 | 1 |
| 1 | F2-3 | 0 |
| 0 | F2-2 | 1 |

C. RAM

1. Perform the CAT Box preliminary set-up.

2. Set the CAT Box switches as follows:
 - a. Press TESTER RESET
 - b. DBUS SOURCE: ADDR
 - c. BYTES: 1024
 - d. R/W MODE: (OFF)
 - e. R/W: WRITE
 - f. Enter 0000 on the keypad
 - g. Toggle R/W MODE to PULSE and back to (OFF)
 - h. R/W: READ
 - i. Toggle R/W MODE to PULSE and back to (OFF)
3. If the CAT Box reads an address that doesn't compare, the COMPARE ERROR LED lights up, the ADDRESS/SIGNATURE display shows the failing address location, and the ERROR DATA DISPLAY switch is enabled. Using this switch, determine if the error is in the high- or low-order RAM.
4. Repeat the test with DBUS SOURCE set to ADDR.
5. Repeat steps 2-4, entering 0400 on the keypad (step f).
6. Repeat steps 2-4, entering 2000 on the keypad (step f).
7. Repeat steps 2-4, entering 2400 on the keypad (step f).
8. Repeat steps 2-4, entering 2800 on the keypad (step f).
9. Repeat steps 2-4, entering 2C00 on the keypad (step f).

D. Option Switch Inputs

1. Perform the CAT Box preliminary set-up.
2. BYTES: 1
3. R/W: READ
4. R/W MODE: (OFF)
5. Key in 0D00
6. R/W MODE: STATIC
7. Activate the option switches at location N13 while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the switches are operating properly.
8. Repeat steps 4-7, entering 0E00 in step 5, and activate switches at location L12.

E. Custom Audio I/O Chips

NOTE: Tempest™ has two custom audio I/O chips. Each must be tested separately. There are several ways to test the chips:

- Perform the Self-Test.
- Substitute good part for defective part.
- Use the procedure that follows.

1. Perform the CAT Box preliminary set-up.
2. BYTES: 1
3. R/W: WRITE
4. R/W MODE: (OFF)
5. Enter address from Figure 3
6. Press DATA SET
7. Enter the data from Figure 3
8. R/W MODE to PULSE and back to (OFF)
9. Repeat steps 5-8 for each address and data, noting the test results.



Figure 3 Custom Audio I/O Chips

| ADDRESS | DATA | TEST RESULTS |
|---------|------|--|
| 60CF | 00 | Custom Audio I/O Chip #1 channel 1 produces pure tone. |
| 60CF | 03 | |
| 60C0 | 55 | |
| 60C1 | AF | |
| 60C1 | 00 | Custom Audio I/O Chip #1 channel 1 off. |
| 60C2 | 55 | Custom Audio I/O Chip #1 channel 2 produces pure tone. |
| 60C3 | AF | |
| 60C3 | 00 | Custom Audio I/O Chip #1 channel 2 off. |
| 60C4 | 55 | Custom Audio I/O Chip #1 channel 3 produces pure tone. |
| 60C5 | AF | |
| 60C5 | 00 | Custom Audio I/O Chip #1 channel 3 off. |
| 60C6 | 55 | Custom Audio I/O Chip #1 channel 4 produces pure tone. |
| 60C7 | AF | |
| 60C7 | 00 | Custom Audio I/O Chip #1 channel 4 off. |

| ADDRESS | DATA | TEST RESULTS |
|---------|------|--|
| 60DF | 00 | Custom Audio I/O Chip #2 channel 1 produces pure tone. |
| 60DF | 03 | |
| 60D0 | 55 | |
| 60D1 | AF | |
| 60D1 | 00 | Custom Audio I/O Chip #2 channel 1 off. |
| 60D2 | 55 | Custom Audio I/O Chip #2 channel 2 produces pure tone. |
| 60D3 | AF | |
| 60D3 | 00 | Custom Audio I/O Chip #2 channel 2 off. |
| 60D4 | 55 | Custom Audio I/O Chip #2 channel 3 produces pure tone. |
| 60D5 | AF | |
| 60D5 | 00 | Custom Audio I/O Chip #2 channel 3 off. |
| 60D6 | 55 | Custom Audio I/O Chip #2 channel 4 produces pure tone. |
| 60D7 | AF | |
| 60D7 | 00 | Custom Audio I/O Chip #2 channel 4 off. |

F. Player Input Switches and Encoder Wheel

1. Perform the CAT Box Preliminary Set-up
2. DBUS SOURCE to DATA
3. BYTES: 256
4. R/W: WRITE
5. R/W MODE: (OFF)
6. Key in 60D0
7. Press DATA SET
8. Key in 00
9. Toggle R/W MODE to PULSE and back to (OFF)
10. BYTES: 1
11. R/W: READ
12. Key in 60D8
13. R/W MODE: STATIC
14. Pushing the following player input switches should cause the DATA DISPLAY to change: FIRE, SUPERZAPPER, 1-player start and 2-player start. (Also Player-2 FIRE and Player-2 SUPERZAPPER in cocktail* games.)

NOTE: For the encoder wheel, repeat the above instructions keying in 60C0 in step 6 and 60C8 in step 12. Turning the encoder wheel should cause the DATA DISPLAY to change.

*To test player-2 inputs in cocktail games connect IC D6-1 to + 5.

G. LED and Coin Counter Outputs

1. Perform the CAT Box Preliminary set-up.
2. DBUS SOURCE to DATA
3. BYTES: 1
4. R/W: WRITE
5. R/W MODE: (OFF)
6. Key in address from Figure 4
7. Press DATA SET
8. Key in on or off data from Figure 4
9. R/W MODE to STATIC and back to (OFF)
10. Repeat steps 6-9 to turn off coin counter solenoids, or to test another address.

If you write data that activates a solenoid, deactivate it by pressing the reset button on the game board or by writing "off" data. If you leave a solenoid activated for more than about 10 seconds it will over-heat and may have to be replaced.

Figure 4 LED and Coin Counter Addresses

| ADDRESS | ON-DATA | OFF-DATA | OUTPUT NAME |
|---------|---------|----------|---------------------|
| 4000 | 01 | 00 | Right Coin Counter |
| 4000 | 02 | 00 | Center Coin Counter |
| 4000 | 04 | 00 | Left Coin Counter |
| 60E0 | FD | FF | 1-player start LED |
| 60E0 | FE | FF | 2-player start LED |

H. Analog Vector-Generator

1. Test:

1. Perform CAT Box preliminary set-up.
2. DATA SOURCE: DATA
3. R/W: WRITE
4. R/W MODE: (OFF)
5. Key in address from Figure 5 or press ADDRESS INC.
6. Press DATA SET
7. Key in data from Figure 5
8. Set R/W MODE to PULSE and then to (OFF)
9. Repeat steps 5-8 for each address in Figure 5

CAUTION

You may damage the circuitry of the X-Y monitor if you key in the VG GO signal without first checking all the addresses and data. Check the data by reading each address location using steps 10-14:

10. R/W: READ
11. R/W MODE: (OFF)
12. Key in address or press ADDRESS INC.
13. R/W MODE: PULSE
14. Check the data in the DATA DISPLAY against the data in Figure 5

If you are sure the data is correct, proceed to steps 15-19:

15. R/W MODE: WRITE
16. R/W: (OFF)
17. Key in VG GO address (4800 for TEMPEST™)
18. R/W to PULSE and then back to (OFF)
19. After writing to the VG GO address, the monitor should show a large plus sign. Failure of the horizontal or vertical circuits shows up as a single line drawn on the monitor. *If your monitor does not display a large plus sign, contact Atari Field Service.*

Figure 5 Analog Vector-Generator Data

| Address | Data | Address | Data | Address | Data |
|---------|------|---------|------|---------|------|
| 2000 | 40 | 200C | FF | 2018 | 00 |
| 2001 | 80 | 200D | 03 | 2019 | 40 |
| 2002 | 00 | 200E | 00 | 201A | 80 |
| 2003 | 70 | 200F | 62 | 201B | 00 |
| 2004 | 00 | 2010 | 40 | 201C | 80 |
| 2005 | 1E | 2011 | 80 | 201D | 1F |
| 2006 | 00 | 2012 | 80 | 201E | 00 |
| 2007 | 1E | 2013 | 00 | 201F | 00 |
| 2008 | 00 | 2014 | 00 | 2020 | FF |
| 2009 | 60 | 2015 | 00 | 2021 | 40 |
| 200A | FF | 2016 | 01 | 2022 | 00 |
| 200B | 03 | 2017 | 1F | 2023 | E0 |

4 Troubleshooting




With Signature Analysis

A. Signature Analysis Set-up

1. Perform the CAT Box Preliminary set-up.
2. Connect the three BNC to E-Z clip cables (supplied with the CAT Box) to the SIGNATURE ANALYSIS CONTROL START, STOP and CLOCK jacks on the CAT Box.
3. Attach the three black E-Z clips to a ground loop on the Tempest™ game PCB.
4. Attach the CAT Box data probe to the DATA jack on the CAT Box.
5. The colored E-Z clips on the cables will be moved about for each group of signatures to be taken.
6. Set the CAT Box switches as follows:
 - TESTER MODE: SIG
 - TESTER SELF-TEST: OFF
 - PULSE MODE: LATCHED
 - START: As indicated
 - STOP: As indicated
 - CLOCK: As indicated
7. Power up the game board and the CAT Box.

B. Address Lines

1. CAT Box Settings for Address Bus Test

| Probe | Trigger | IC-Pin | Test Pt. |
|-------|---|--------|----------|
| Start |  | A6-3 | |
| Stop |  | A6-3 | |
| Clock |  | C2-39 | Φ2 |

Verify CAT Box settings and connections as follows:

- probe GND test point = 0000 signature
- probe +5V test point = 0001 signature




2. Signatures

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|-----------------------|-------------|---------------------|
| B/C1-12 | AB0 | UUUU |
| B/C1-14 | AB1 | 5555 |
| B/C1-16 | AB2 | CCCC |
| B/C1-18 | AB3 | 7F7F |
| B/C1-9 | AB4 | 5H21 |
| B/C1-7 | AB5 | 0AFA |
| B/C1-5 | AB6 | UPFH |
| B/C1-3 | AB7 | 52F8 |
| A/B1-12 | AB8 | HC89 |
| A/B1-14 | AB9 | 2H70 |
| A/B1-16 | AB10 | HPP0 |
| A/B1-18 | AB11 | 1293 |
| A/B1-3 | AB12 | HAP7 |
| B3-2 | A13 | 3C96 |
| B3-3 | A14 | 3827 |
| B3-1 | A15 | 755U |
| A6-4 | A15 | 755P |

C. Address Decoder

NOTE: While testing decoders and ROMs, it may be necessary to add 270 pF capacitors to ADDR 12, 13, 14 and 15 to eliminate unstable signatures.

1. CAT Box Settings for Address Decoder Test




| Probe | Trigger | IC-Pin | Test Pt. |
|-------|---|--------|----------|
| Start |  | A6-3 | |
| Stop |  | A6-3 | |
| Clock |  | | Φ2 |

2. Signatures

NOTE: To obtain Signatures from IC J5, ground R/ \overline{W} testpoint.

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|-----------------------|--------------------|---------------------|
| B3-7 | $\overline{I/O}$ | F2A6 |
| E3-2 | $\overline{I/O}$ | F2A7 |
| F3-8 | $\overline{EI/O}$ | F2A6 |
| J5-9 | \overline{VGRST} | 5969 |
| J5-10 | \overline{WDCLR} | 0PC5 |
| J5-11 | \overline{VGGO} | 270P |
| J5-12 | $\overline{BB^*}$ | 9CH2 |
| B3-5 | \overline{VMEM} | 12U3 |
| B3-4 | $\overline{AA^*}$ | 4P0A |
| J2-7 | $\overline{ROM8}$ | 56C3 |
| J2-6 | $\overline{ROM7}$ | 8019 |
| J2-5 | $\overline{ROM6}$ | 5AH1 |
| J2-4 | $\overline{ROM5}$ | 9HUC |
| J2-9 | $\overline{ROM4}$ | 1920 |
| J2-10 | $\overline{ROM3}$ | C34C |
| J2-11 | $\overline{ROM2}$ | 597C |
| J2-12 | $\overline{ROM1}$ | UA87 |
| C1-7 | $\overline{ROM0}$ | 4154 |
| C1-6 | \overline{ROMX} | 960F |

3. CAT Box Settings for Address Decoder Test

| Probe | Trigger | Testpoint |
|-------|---|-----------|
| Start |  | A6-4 |
| Stop |  | A6-4 |
| Clock |  | Φ2 |

4. Signatures

Verify CAT Box setting and connections as follows:
probe +5V = 755U signature.




| Logic Probe on IC-Pin | Signature Should Be |
|-----------------------|---------------------|
| B3-9 | 970C |
| B3-10 | 868C |
| B3-11 | 7FF8 |
| B3-12 | 1817 |

D. ROM and Data Lines

NOTE: When taking signatures on ROMs, install a 270 pF capacitor between IC B3, Pin 2 and ground.

1. CAT Box Settings for ROMX Test

(I.C. D1 for ROM part no. 136002-101, -113 or -133.)




| Probe | Trigger | Testpoint |
|-------|---|--------------------------|
| Start |  | $\overline{\text{ROMX}}$ |
| Stop |  | $\overline{\text{ROMX}}$ |
| Clock |  | $\phi 2$ |

2. Signatures

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|-----------------------|-------------|---------------------|
| D1-9 | DB0 | 1F4H |
| D1-10 | DB1 | 4P55 |
| D1-11 | DB2 | P2C5 |
| D1-13 | DB3 | UH32 |
| D1-14 | DB4 | 4HFA |
| D1-15 | DB5 | 0P76 |
| D1-16 | DB6 | 86CP |
| D1-17 | DB7 | P29C |

3. CAT Box Settings for ROM0 Test

(I.C. E1 for ROM part no. 136002-102 or -114.
I.C. D1 for ROM part no. 136002-133.)

| Probe | Trigger | Testpoint |
|-------|---|--------------------------|
| Start |  | $\overline{\text{ROM0}}$ |
| Stop |  | $\overline{\text{ROM0}}$ |
| Clock |  | $\phi 2$ |




4. Signatures

Verify CAT Box settings and connections as follows:
probe + 5V = 7A70 signature.

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|-----------------------|-------------|---------------------|
| E1-9 | DB0 | 6481 |
| E1-10 | DB1 | P6A9 |
| E1-11 | DB2 | 9552 |
| E1-13 | DB3 | 40F3 |
| E1-14 | DB4 | 37C2 |
| E1-15 | DB5 | 0A18 |
| E1-16 | DB6 | A2C0 |
| E1-17 | DB7 | 9HC5 |

5. CAT Box Settings for ROM1 Test

(I.C. F1 for ROM part no. 136002-103, 115 or -134.)

| Probe | Trigger | Testpoint |
|-------|---|--------------------------|
| Start |  | $\overline{\text{ROM1}}$ |
| Stop |  | $\overline{\text{ROM1}}$ |
| Clock |  | $\phi 2$ |




6. Signatures

Verify CAT Box settings and connections as follows:
probe + 5V = 7A70 signature.

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|-----------------------|-------------|---------------------|
| F1-9 | DB0 | 3892 |
| F1-10 | DB1 | 01U5 |
| F1-11 | DB2 | PH6P |
| F1-13 | DB3 | UP9F |
| F1-14 | DB4 | UP44 |
| F1-15 | DB5 | CA33 |
| F1-16 | DB6 | 3U05 |
| F1-17 | DB7 | 8CP3 |

7. CAT Box Settings for ROM2 Test

(I.C. H1 for ROM part no. 136002-104 or -116.
I.C. F1 for ROM part no. 136002-134.)

| Probe | Trigger | Testpoint |
|-------|---|--------------------------|
| Start |  | $\overline{\text{ROM2}}$ |
| Stop |  | $\overline{\text{ROM2}}$ |
| Clock |  | $\phi 2$ |




8. Signatures

Verify CAT Box settings and connections as follows:
probe + 5V = 7A70 signature.

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|-----------------------|-------------|---------------------|
| H1-9 | DB0 | 7550 |
| H1-10 | DB1 | A01F |
| H1-11 | DB2 | A540 |
| H1-13 | DB3 | 5U60 |
| H1-14 | DB4 | 2068 |
| H1-15 | DB5 | 9767 |
| H1-16 | DB6 | 54CA |
| H1-17 | DB7 | 7F8F |

9. CAT Box Settings for ROM3 Test




(I.C. J1 for ROM part no. 136002-105, -117 or -135.)

| <i>Probe</i> | <i>Trigger</i> | <i>Testpoint</i> |
|--------------|---|------------------|
| Start |  | <u>ROM3</u> |
| Stop |  | ROM3 |
| Clock |  | φ2 |

10. SignaturesVerify CAT Box settings and connections as follows:
probe +5V = 7A70 signature.

| <i>Logic Probe on IC-Pin</i> | <i>Signal Name</i> | <i>Signature Should Be</i> |
|----------------------------------|------------------------|--------------------------------|
| J1-9 | DB0 | 09A6 |
| J1-10 | DB1 | 6A12 |
| J1-11 | DB2 | 91CA |
| J1-13 | DB3 | 10HP |
| J1-14 | DB4 | F53U |
| J1-15 | DB5 | C67C |
| J1-16 | DB6 | 8272 |
| J1-17 | DB7 | F651 |

11. CAT Box Settings for ROM4 Test(I.C. K1 for ROM part no. 136002-106 or -118.
I.C. J1 for ROM part no. 136002-135.)




| <i>Probe</i> | <i>Trigger</i> | <i>Testpoint</i> |
|--------------|---|------------------|
| Start |  | <u>ROM4</u> |
| Stop |  | ROM4 |
| Clock |  | φ2 |

12. SignaturesVerify CAT Box settings and connections as follows:
probe +5V = 7A70 signature.

| <i>Logic Probe on IC-Pin</i> | <i>Signal Name</i> | <i>Signature Should Be</i> |
|----------------------------------|------------------------|--------------------------------|
| K1-9 | DB0 | A8FU |
| K1-10 | DB1 | U3U7 |
| K1-11 | DB2 | C8CH |
| K1-13 | DB3 | 353F |
| K1-14 | DB4 | 93FU |
| K1-15 | DB5 | UFH1 |
| K1-16 | DB6 | A165 |
| K1-17 | DB7 | 5399 |

13. CAT Box Settings for ROM5 Test




(I.C. L/M1 for ROM part no. 136002-107, -119 or -136.)

| <i>Probe</i> | <i>Trigger</i> | <i>Testpoint</i> |
|--------------|---|------------------|
| Start |  | <u>ROM5</u> |
| Stop |  | ROM5 |
| Clock |  | φ2 |

14. SignaturesVerify CAT Box settings and connections as follows:
probe +5V = 7A70 signature.

| <i>Logic Probe on IC-Pin</i> | <i>Signal Name</i> | <i>Signature Should Be</i> |
|----------------------------------|------------------------|--------------------------------|
| L/M1-9 | DB0 | 4876 |
| L/M1-10 | DB1 | 5397 |
| L/M1-11 | DB2 | 7396 |
| L/M1-13 | DB3 | C9CH |
| L/M1-14 | DB4 | HF73 |
| L/M1-15 | DB5 | 11U6 |
| L/M1-16 | DB6 | 43C8 |
| L/M1-17 | DB7 | 2P85 |

15. CAT Box Settings for ROM6 Test(I.C. M/N1 for ROM part no. 136002-108 or -120.
I.C. L/M1 for ROM part no. 136002-136.)




| <i>Probe</i> | <i>Trigger</i> | <i>Testpoint</i> |
|--------------|---|------------------|
| Start |  | <u>ROM6</u> |
| Stop |  | ROM6 |
| Clock |  | φ2 |

16. SignaturesVerify CAT Box settings and connections as follows:
probe +5V = 7A70 signature.

| <i>Logic Probe on IC-Pin</i> | <i>Signal Name</i> | <i>Signature Should Be</i> |
|----------------------------------|------------------------|--------------------------------|
| M/N-9 | DB0 | A4AC |
| M/N-10 | DB1 | 3A7C |
| M/N-11 | DB2 | 0F22 |
| M/N-13 | DB3 | H221 |
| M/N-14 | DB4 | 2H07 |
| M/N-15 | DB5 | 818A |
| M/N-16 | DB6 | 1699 |
| M/N-17 | DB7 | 4149 |

17. CAT Box Settings for ROM7 Test

(I.C. P1 for ROM part no. 136002-109, -121 or -137.)

| Probe | Trigger | Testpoint |
|-------|---|-----------|
| Start |  | ROM7 |
| Stop |  | ROM7 |
| Clock |  | Φ 2 |




18. Signatures

Verify CAT Box settings and connections as follows:
probe +5V = 7A70 signature.

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|--------------------------|----------------|------------------------|
| P1-9 | DB0 | P4F3 |
| P1-10 | DB1 | 2C06 |
| P1-11 | DB2 | 4614 |
| P1-13 | DB3 | 7A63 |
| P1-14 | DB4 | 434C |
| P1-15 | DB5 | 3C66 |
| P1-16 | DB6 | P8U6 |
| P1-17 | DB7 | 2C3A |

19. CAT Box Settings for ROM8 Test

(I.C. R1 for ROM part no. 136002-110 or -122.
I.C. P1 for ROM part no. 136002-137.)

| Probe | Trigger | Testpoint |
|-------|---|-----------|
| Start |  | ROM8 |
| Stop |  | ROM8 |
| Clock |  | Φ 2 |

20. Signatures




Verify CAT Box settings and connections as follows:
probe +5V = 7A70 signature.

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|--------------------------|----------------|------------------------|
| R1-9 | DB0 | 9HFP |
| R1-10 | DB1 | U7HH |
| R1-11 | DB2 | F32H |
| R1-13 | DB3 | F66U |
| R1-14 | DB4 | U379 |
| R1-15 | DB5 | 490P |
| R1-16 | DB6 | 5P99 |
| R1-17 | DB7 | CFA8 |

21. CAT Box Settings for Vector

ROM Test (I.C. N/P3 for part no. 136002-111, -123 or -138.)

NOTE: When taking signatures on IC N/P3, ground IC-Pin B3-5.

| Probe | Trigger | IC-Pin | Testpoint |
|-------|---|--------|-----------|
| Start |  | C1-10 | |
| Stop |  | C1-10 | |
| Clock |  | | Φ 2 |

22. Signatures




Verify CAT Box settings and connections as follows:
probe +5V = 7A70 signature.

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|--------------------------|----------------|------------------------|
| N/P3-9 | DB0 | H1U9 |
| N/P3-10 | DB1 | 5U8C |
| N/P3-11 | DB2 | 0C59 |
| N/P3-13 | DB3 | 507P |
| N/P3-14 | DB4 | 2A8P |
| N/P3-15 | DB5 | 9F0C |
| N/P3-16 | DB6 | AH97 |
| N/P3-17 | DB7 | 29AH |

23. CAT Box Settings for Vector

ROM1 Test (I.C. R3 for part no. 136002-112 or -124.)

NOTE: When taking signatures on I.C. R3, ground IC-Pin B3-5.

| Probe | Trigger | IC-Pin | Testpoint |
|-------|---|----------|-----------|
| Start |  | C1 Pin 9 | |
| Stop |  | C1 Pin 9 | |
| Clock |  | | Φ 2 |

24. Signatures

| Logic Probe on IC-Pin | Signal Name | Signature Should Be |
|--------------------------|----------------|------------------------|
| R3-9 | DB0 | 3FH3 |
| R3-10 | DB1 | 0H59 |
| R3-11 | DB2 | 9H5H |
| R3-13 | DB3 | 98PF |
| R3-14 | DB4 | PA27 |
| R3-15 | DB5 | 5U3H |
| R3-16 | DB6 | 97FC |
| R3-17 | DB7 | 583A |

E. Math Box

The Math Box signature analysis procedure is somewhat different from other procedures, so follow these set-up instructions for the three tests carefully.

In addition to your CAT Box or signature analyzer, you'll need an SA Harness Assembly. Order Atari part number A036836-01 or see Figure 6 to make your own.

A. Math Box Test #1 Procedure:

1. Plug SA Harness Assembly Test #1 connector onto Signature Analyzer connector (J16) on the Auxiliary PCB.
2. Connect the CAT Box Start, Stop and Clock E-Z hooks to the SA Harness Assembly as shown in Figure 7.
3. On the main PCB, connect PWR ON RESET test point to ground, and power-up the game and the CAT Box.
4. Don't remove the microprocessor (6502A) from the main PCB.

Don't connect the 50 pin ribbon cable to the main PCB edge connector.

Don't connect W DOG DIS to ground.

5. Set the CAT Box switches as follows:

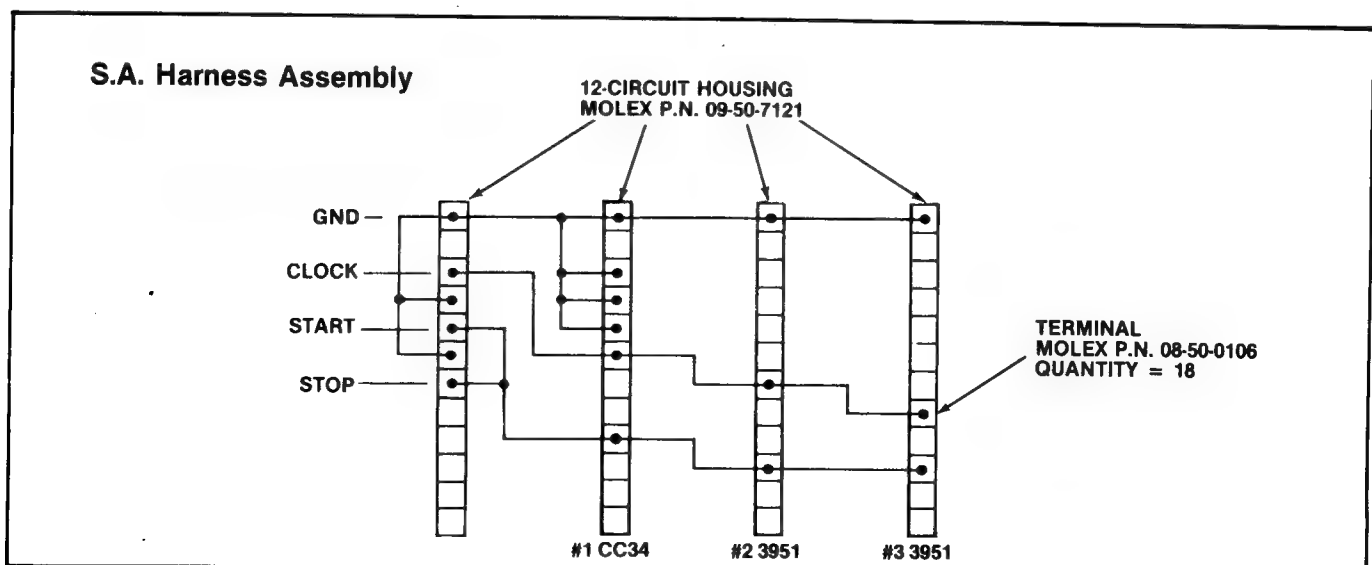
- a. START ☐
- b. STOP ☐
- c. CLOCK ☐
- d. TESTER MODE: SIG
- e. Press TESTER RESET

6. With the logic probe touching the +5V test point on the Auxiliary PCB, the ADDRESS/SIGNATURE display should read CC34. This will verify that your test set-up is correct. If you don't get CC34, recheck your set-up.

NOTE: Signatures are listed in the order that they should be done. As often as possible, *IC-Pin* refers to a chip output. As a general rule, when a bad signature is discovered, the IC listed in the *IC-Pin* column can be suspected as faulty.

Those signatures marked with an asterisk (*) should be taken with a 1K resistor clipped between the logic probe and the +5V test point.

Figure 6 S.A. Harness Assembly



Signatures




*Logic Probe
on IC-Pin*

*Signature
Should Be*

| | |
|---------|-------|
| C1-11 | H58A |
| C1-12 | 77F7 |
| C1-13 | 85PA |
| C1-14 | 7P25 |
| D1-11 | 5CP0 |
| D1-12 | P5PH |
| D1-13 | 725C |
| D1-14 | 96PF |
| F1-12 | 4PPF |
| F1-11 | OUF0 |
| F1-10 | 3CAP |
| F1-9 | A6A3 |
| H1-12 | 26A6 |
| H1-11 | 91HA |
| H1-10 | P9C1 |
| H1-9 | 2987 |
| J1-12 | 96U0 |
| J1-11 | UC59 |
| J1-10 | 6989 |
| J1-9 | 3FU4 |
| K1-12 | 05A6 |
| K1-11 | 60H6 |
| K1-10 | PPF6 |
| K1-9 | 34C2 |
| L1-12 | 58A1 |
| L1-11 | 1AA2 |
| L1-10 | F74F |
| L1-9 | 6CF6 |
| E1-12 | F765 |
| E1-11 | CPU8 |
| E1-10 | 0000 |
| E1-9 | F515 |
| F4-2 | CC34 |
| E4-6 | A6A3 |
| A2-6 | 0000 |
| B1-2 | 8A7H |
| B1-5 | CU2P |
| B1-6 | 1C6C |
| B1-9 | 6U30 |
| B1-12 | 5AAH |
| B1-15 | 03A7 |
| B1-16 | 9A08 |
| B1-19 | 2327 |
| K/L2-33 | 6PUP |
| K/L2-16 | 9AFH* |
| K/L2-8 | 809A* |
| F/H2-33 | 9CPP |
| F/H2-16 | 11C5* |

| | |
|--------|-------|
| F/H2-8 | 78AA* |
| J2-33 | 8631 |
| J2-16 | 11C5* |
| J2-8 | 7U19* |
| E2-34 | A1F7 |
| E2-31 | 1781 |
| E2-16 | 9AFH* |
| E5-11 | C646 |
| D4-8 | 0600 |
| E4-11 | CC34 |
| F5-11 | C835* |
| D4-6 | C4U4 |
| F5-6 | 753F |
| E4-8 | CPU8 |
| E5-8 | 45A1* |

B. Math Box Test #2A Procedure

1. Plug SA Harness Assembly Test #2 connector on-to Signature Analyzer connector (J16) on the Auxiliary PCB.
2. Connect the CAT Box Start, Stop and Clock E-Z hooks to the SA Harness Assembly as shown in Figure 7.
3. Don't remove the microprocessor (6502A) from the main PCB.
Don't connect the 50 pin ribbon cable to the main PCB edge connector.
Don't connect W DOG DIS to ground.
Don't connect PWR ON RESET to ground.
4. Set the CAT Box switches as follows:
 - a. START 
 - b. STOP 
 - c. CLOCK 
 - d. TESTER MODE: SIG
 - e. Press TESTER RESET
5. Enter the self-test mode and advance the screen with the slam switch until the large blank rectangle appears. This procedure is described in Figure 6, Chapter 2 of the Tempest™ Operation, Maintenance, and Service Manual.
6. With the logic probe touching the +5V test point on the Auxiliary PCB, the ADDRESS/SIGNATURE display should read 3951. This will verify that your test set-up is correct. If you don't get 3951, re-check your set-up.

NOTE: Signatures are listed in the order that they should be done. As often as possible, *IC-Pin* refers to a chip output. As a general rule, when a bad signature is discovered, the IC listed in the *IC-Pin* column can be suspected as faulty.

Signatures

| Logic Probe on IC-Pin | Signature Should Be |
|--------------------------|------------------------|
| A1-14 | F722 |
| A1-13 | C4P5 |
| A1-12 | 6UAC |
| A1-11 | 3441 |
| A1-10 | 2P61 |
| A1-9 | 92F3 |
| A1-7 | A856 |
| A1-6 | 3050 |
| A1-5 | H8F9 |
| A1-4 | 9569 |
| A1-3 | 3U53 |
| A1-2 | 9F47 |
| A1-1 | 4FUF |

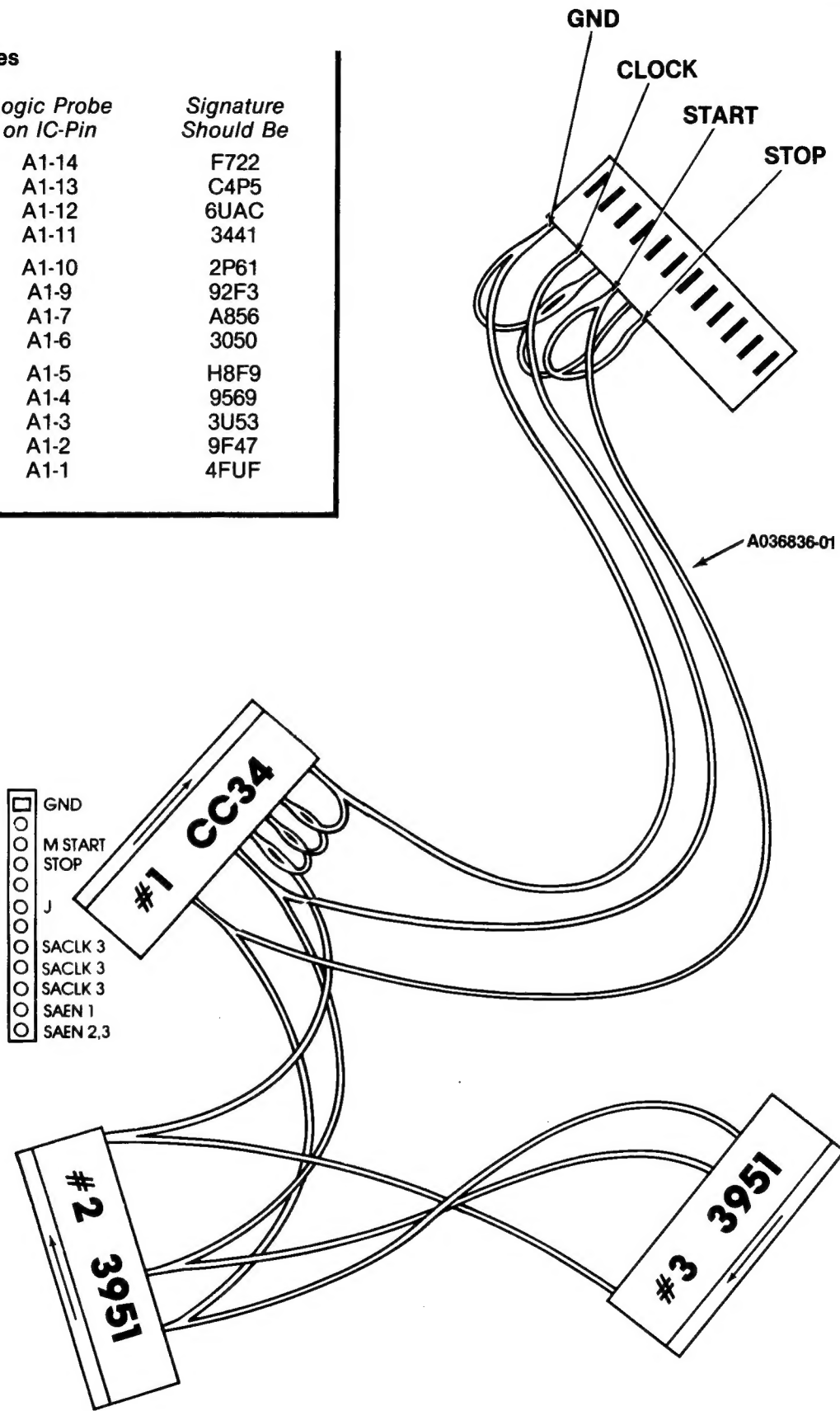





Figure 7 S.A. Harness Assembly

C. Math Box Test #2B Procedure




1. Plug SA Harness Assembly Test #2 connector on-to Signature Analyzer connector (J16) on the Auxiliary PCB.
2. Connect the CAT Box Start, Stop and Clock E-Z hooks to the SA Harness Assembly as shown in Figure 7.
3. Don't remove the microprocessor (6502A) from the main PCB.
Don't connect the 50 pin ribbon cable to the main PCB edge connector.
Don't connect W DOG DIS to ground.
Don't connect PWR ON RESET to ground.
4. Set the CAT Box switches as follows:
 - a. START 
 - b. STOP 
 - c. CLOCK 
 - d. TESTER MODE: SIG
 - e. Press TESTER RESET
5. Enter the self-test mode and advance the screen with the slam switch until the large blank rectangle appears. This procedure is described in Figure 6, Chapter 2 of the Tempest™ Operation, Maintenance, and Service Manual.
6. With the logic probe touching the +5V test point on the Auxiliary PCB, the ADDRESS/SIGNATURE display should read 3951. This will verify that your test set-up is correct. If you don't get 3951, re-check your set-up.

NOTE: Signatures are listed in the order that they should be done. As often as possible, *IC-Pin* refers to a chip output. As a general rule, when a bad signature is discovered, the IC listed in the *IC-Pin* column can be suspected as faulty.

Signatures

| <i>Logic Probe on IC-Pin</i> | <i>Signature Should Be</i> |
|----------------------------------|--------------------------------|
| C1-11 | 92F3 |
| C1-12 | A856 |
| C1-13 | 3050 |
| C1-14 | H8F9 |
| D1-11 | 9569 |
| D1-12 | 3U53 |
| D1-13 | 9F47 |
| D1-14 | 4FUF |

D. Math Box Test #3 Procedure

1. Plug SA Harness Assembly Test #3 connector on-to Signature Analyzer connector (J16) on the Auxiliary PCB.
2. Connect the CAT Box Start, Stop and Clock E-Z hooks to the SA Harness Assembly as shown in Figure 7.
3. Don't remove the microprocessor (6502A) from the main PCB.
Don't connect the 50 pin ribbon cable to the main PCB edge connector.
Don't connect W DOG DIS to ground.
Don't connect PWR ON RESET to ground.
4. Set the CAT Box switches as follows:
 - a. START 
 - b. STOP 
 - c. CLOCK 
 - d. TESTER MODE: SIG
 - e. Press TESTER RESET
5. Enter the self-test mode and advance the screen with the slam switch until the large blank rectangle appears. This procedure is described in Figure 6, Chapter 2 of the Tempest™ Operation, Maintenance, and Service Manual.
6. With the logic probe touching the +5V test point on the Auxiliary PCB, the ADDRESS/SIGNATURE display should read 3951. This will verify that your test set-up is correct. If you don't get 3951, re-check your set-up.

NOTE: Signatures are listed in the order that they should be done. As often as possible, *IC-Pin* refers to a chip output. As a general rule, when a bad signature is discovered, the IC listed in the *IC-Pin* column can be suspected as faulty.

Signatures

| <i>Logic Probe on IC-Pin</i> | <i>Signature Should Be</i> |
|----------------------------------|--------------------------------|
| E2-22 | 1441 |
| E2-23 | 2883 |
| E2-24 | 5107 |
| E2-25 | A20P |
| J2-22 | 441H |
| J2-23 | 883A |
| J2-24 | 1074 |
| J2-25 | 20P9 |



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